R&D Project specification

xEC2: XIMEA Embedded Carrier board V2

For NVIDIA Jetson TX2

Pinout and IO subsystem description

Cabling

Version 1.2, 11/26/2019

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1. xEC2 System

1.1. Overview

XIMEAs xEC2 is a carrier board stack that provides interfaces for powerful and flexible embedded vision units. xEC2 uses the computing capacity of the NVIDIA Jetson TX2 System-on-Module embedded CPU/GPU platform, which provides 4 CPU and 256 GPU cores for parallel data processing. The TX2 module with an optimized Linux-installation is part of the delivery.

As a xiTECH category device, XIMEA offers this carrier boards to realize smart, small and powerful remote or completely autonomous camera-based systems.

1.2. Components

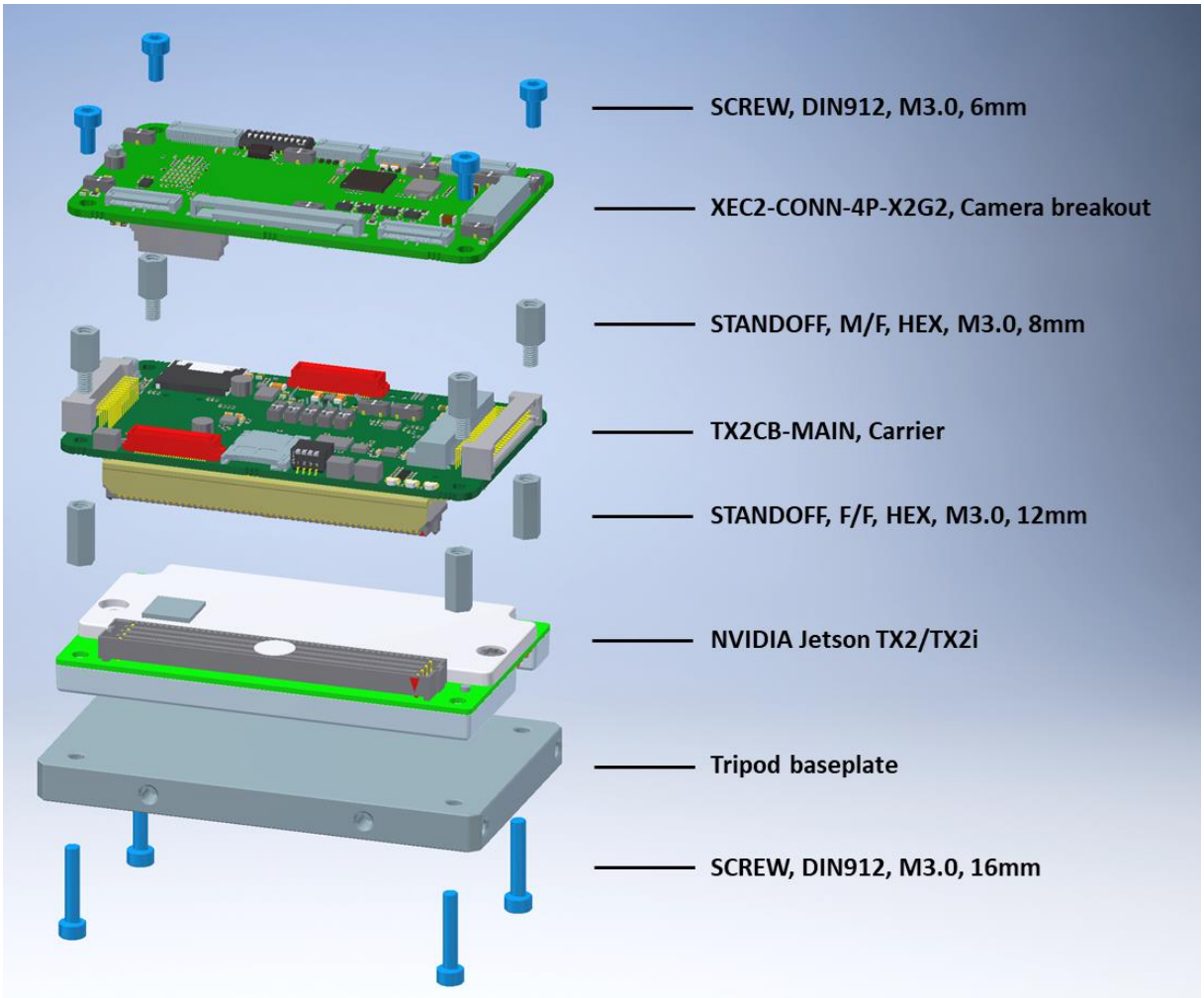


Figure 1-1, XEC2 components (w/o active heatsink)

The xEC2 system consists of the following components:

- Camera breakout board – TX2CB-CONN-4P-X2G2
- Main carrier board – TX2CB-MAIN
- NVIDIA Jetson TX2 / TX2i SoC embedded computer
- Power cable
- Tripod baseplate
- Active heat sink (option)
- Power supply (option)

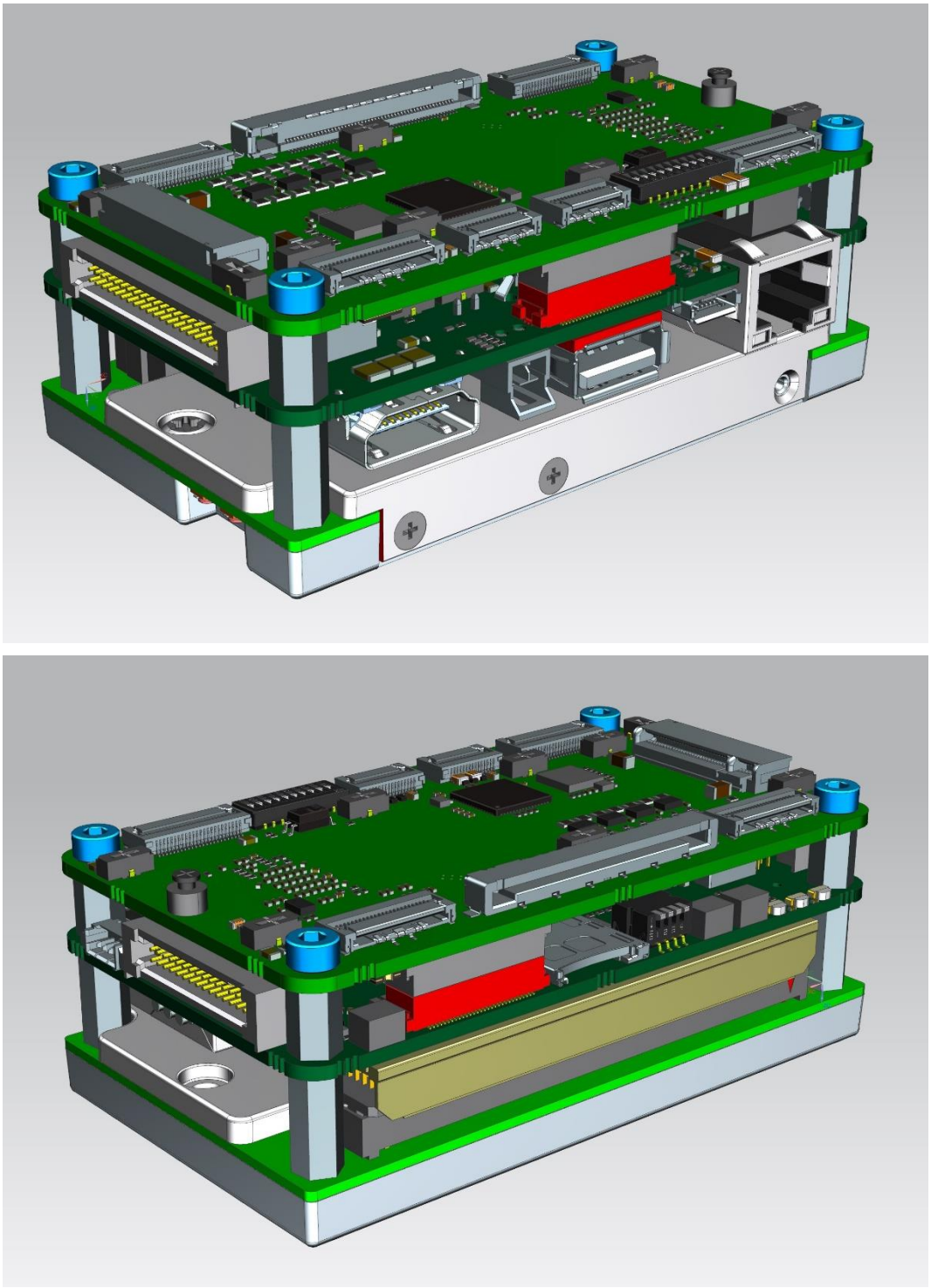


Figure 1-2, XEC2 board stack (w/o baseplate and active heatsink)

1.3. Block diagram

The usable modules and interfaces are distributed on both boards of the XEC2 board stack.

The MAIN-board is directly connected to the TX2 SoC and provides the standard interfaces of the TX2. This board also contains the power supply logic and the IMU.

The CONN-board is connected to the TX2 PCIe system via a PCIe switch module and provides the camera interfaces and the NVMe-SSD interface.

The WIFI ports of the TX2 can be used.

Optionally, an active heat sink can be connected. A connector is available on the MAIN-board to control the fan.

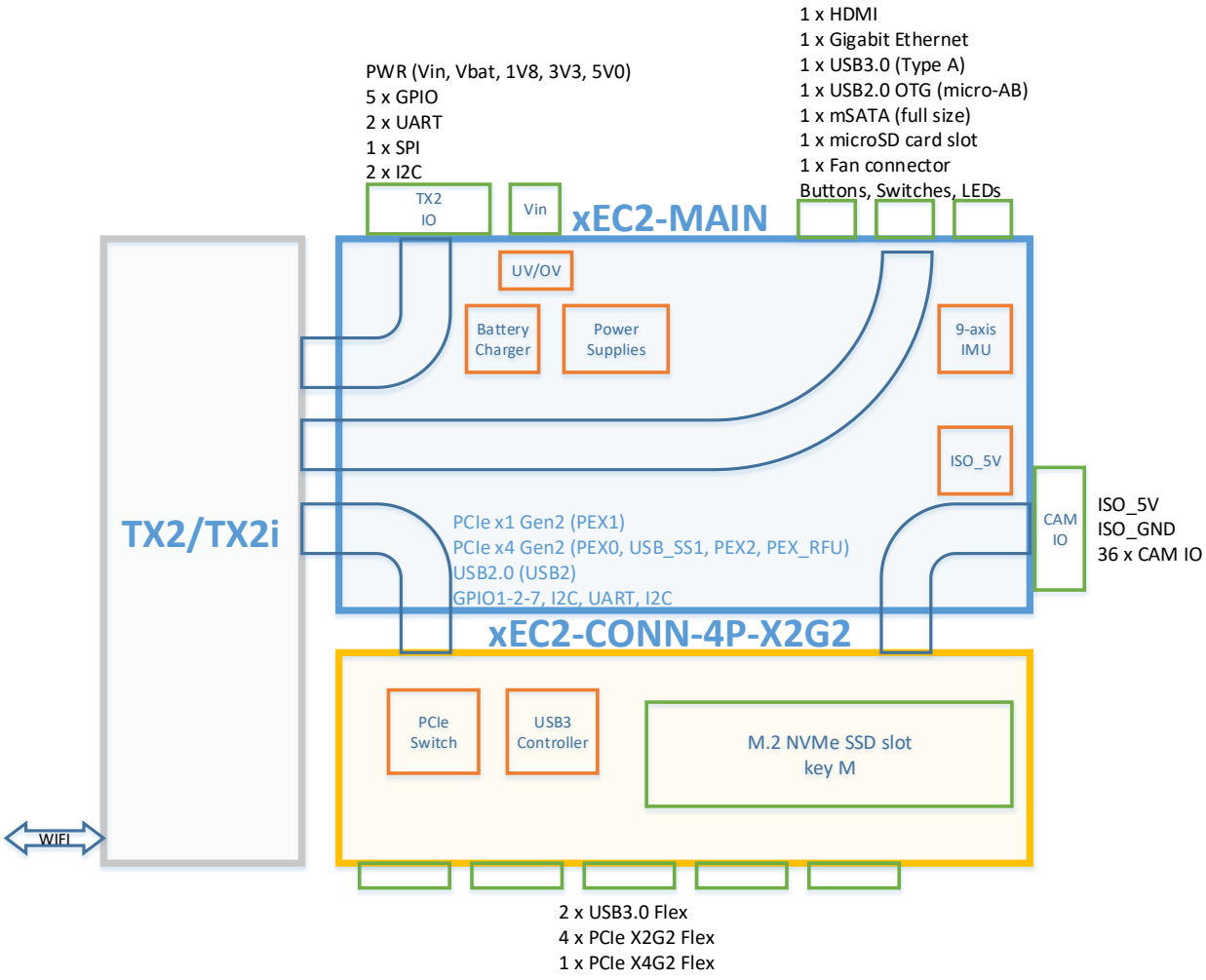


Figure 1-3, XEC2-4P-X2G2 block diagram

1.4. Drawings, dimensions

1.4.1. XEC2-4P-X2G2 system

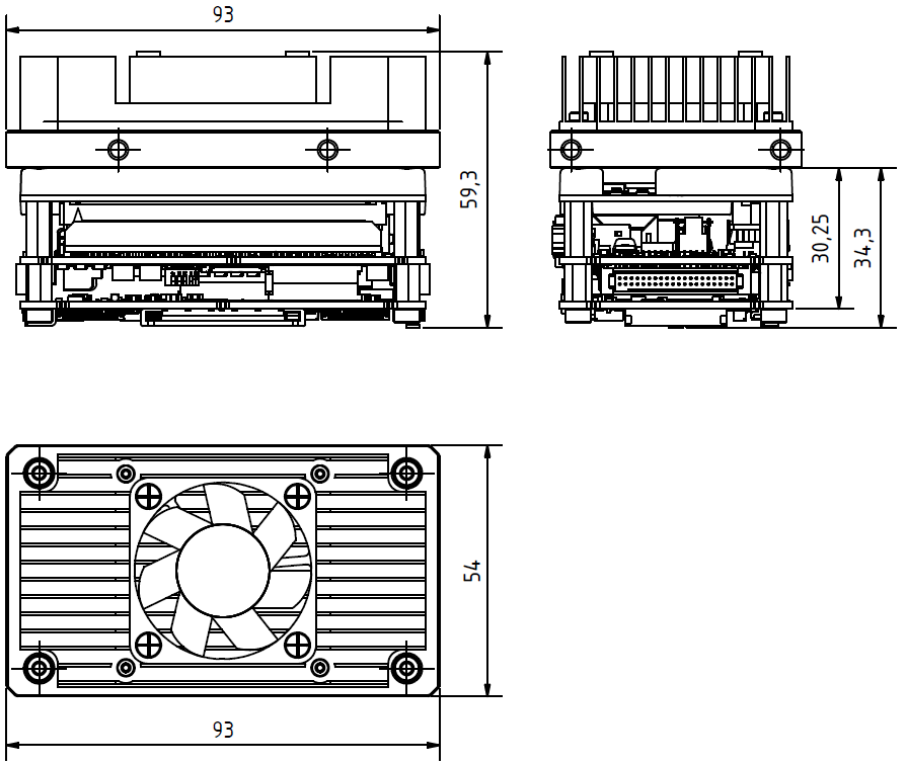


Figure 1-4, dimensions XEC2-4P-X2G2 system with fan / heat sink

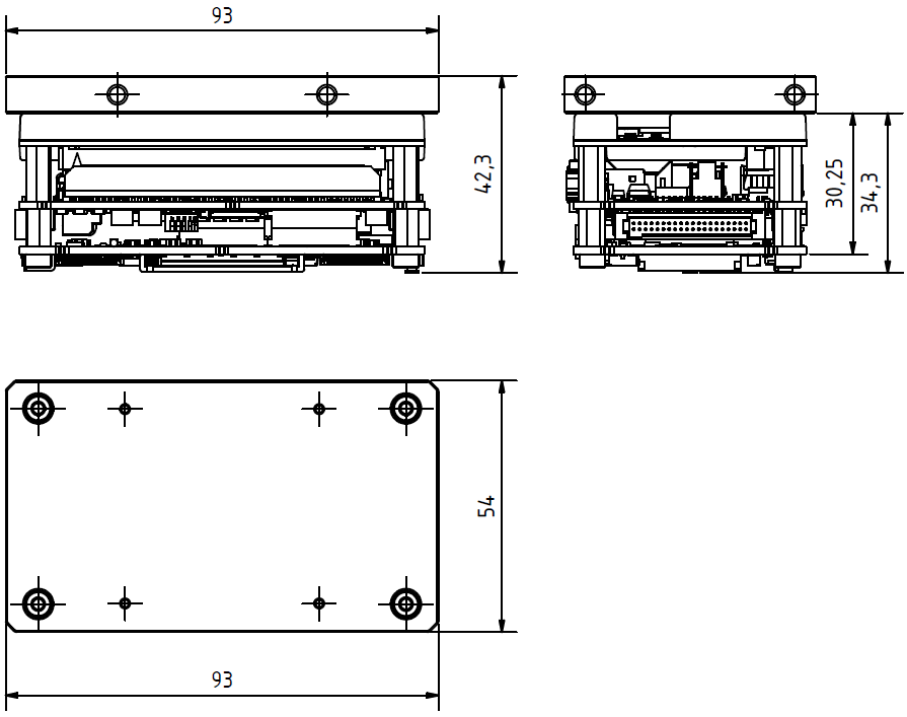


Figure 1-5, dimensions XEC2-4P-X2G2 system without fan / heat sink

1.4.2. TX2CB-MAIN – carrier board

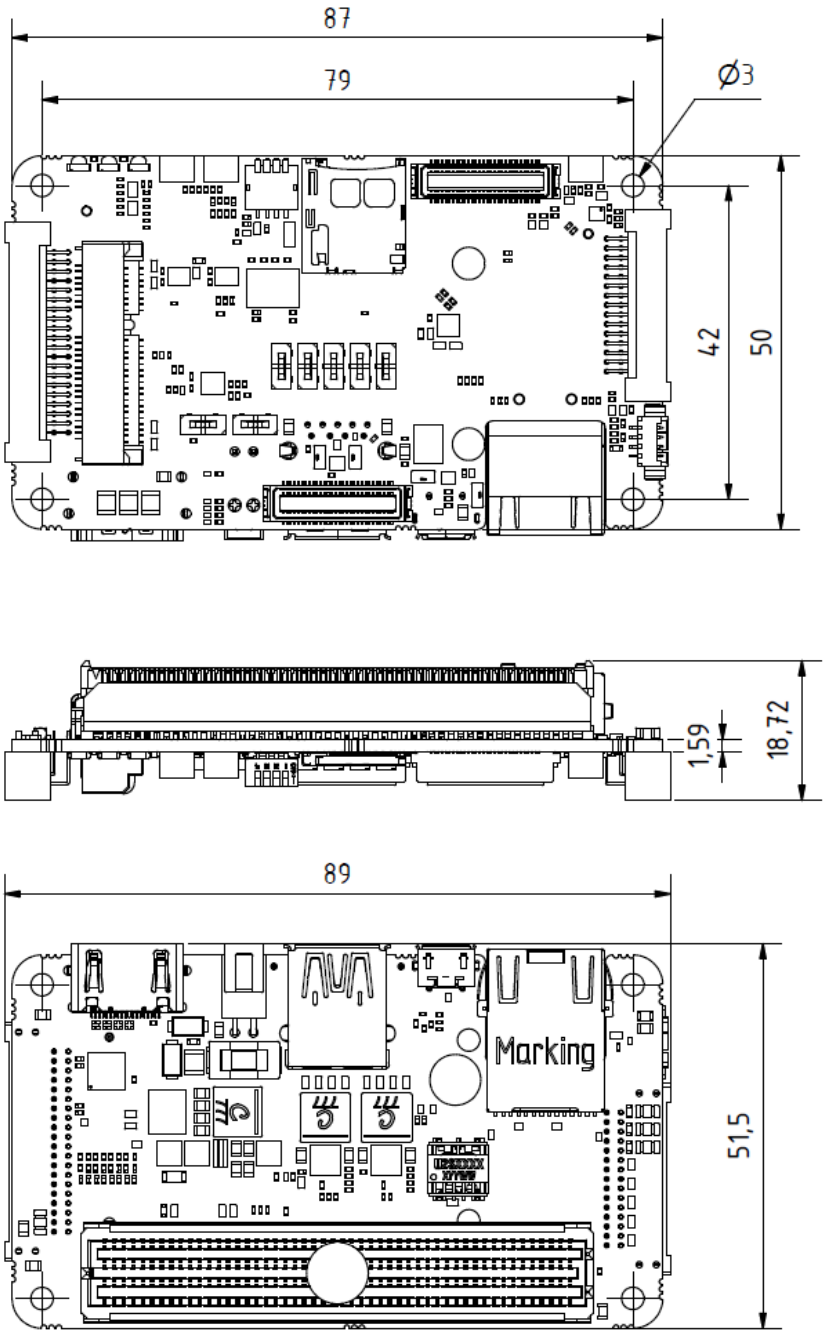


Figure 1-6, dimensions TX2CB-MAIN

1.4.3. TX2CB-CONN-4P-X2G2 – camera board

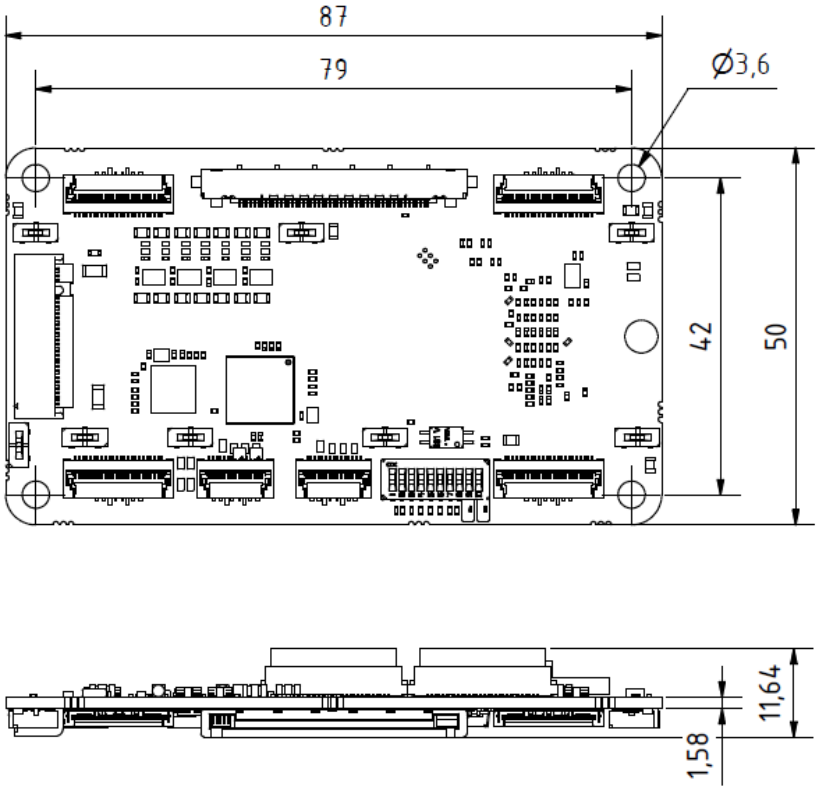


Figure 1-7, dimensions TX2CB-CONN-4P-X2G2

1.4.4. Tripod baseplate

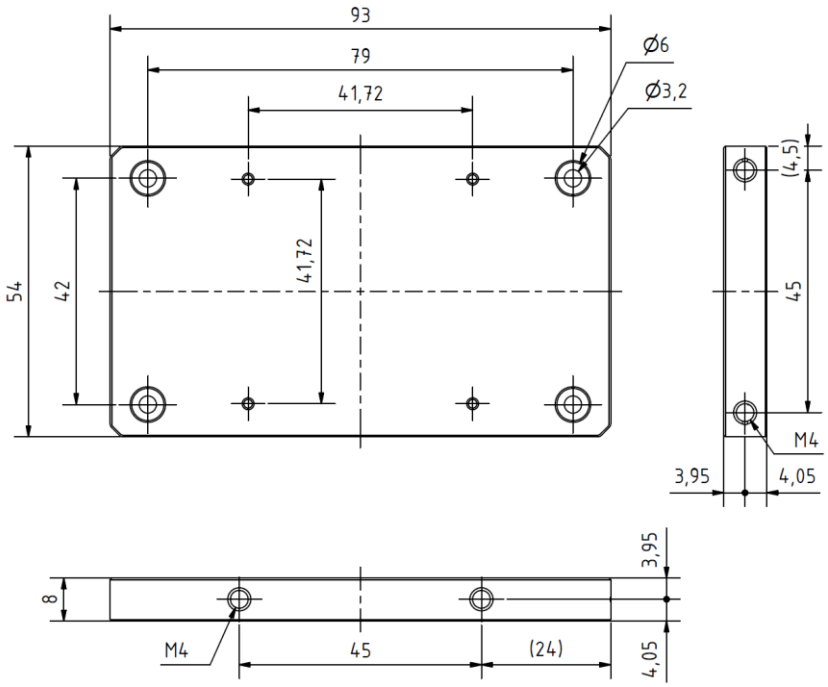


Figure 1-8, dimensions XEC2 tripod baseplate

1.5. General info

1.5.1. Weight

Setup	Weight
pure board stack + TX2, no tripod baseplate / heat sink attached	176 g
pure board stack + TX2 + tripod baseplate	297 g
board stack + TX2, tripod baseplate, active heat sink incl. fan. w/o SD-card, SSD, NVME-SSD, cables, cameras	366 g

Table 1-1, weight

1.5.2. Power supply

The power supply (supplied separately) has should have a nominal voltage of 12V (7 – 19V). The current must be <= 8A.

It might be recommended to connect a 15 V power supply when using the battery charging function. When using an external battery, the power supply voltage must be higher than the battery charging voltage in order to charge the battery. For example, 3S LiPo battery is charged with 3x4.2V=12.6V, thus a 12V power supply won't be able to fully recharge the battery. Instead a 15V power supply should be used in this case.

1.5.3. Power consumption

component	Power consumption
Board-stack (w/o TX2)	< 1W, dependent on the input voltage level
NVIDIA Jetson TX2	dependent on the CPU / GPU load 0.5 – 15 W
SD-Card, M2.SSD, NVMe-SSD, connected USB devices to MAIN board	dependent on model
+ camera(s)	dependent on model
+ active CANON-EF-Mount attached lenses (if applicable)	dependent on model

Table 1-2, power consumption

1.6. NVIDIA Jetson module compatibility

The XEC2 board stack is compatible to NVIDIA Jetson TX2 and TX2i SoC embedded systems.

1.7. Order info / Accessories

The part number of the components are:

Part-#	description
XEC2-4P-X2G2	XEC2 board stack: TX2, MAIN- and COMM-board, tripod baseplate, power cable
XEC2-FAN-COOLER-KIT	active heatsink with fan for xEC2 embedded system
PSU-GSM60B12-P1J	desktop power supply (60W, 12V) - kit with power cord (EU or US)
PSU-GSM60A15-P1J	desktop power supply (60W, 15V) - kit with power cord (EU or US)
MECH-60MM-BRACKET-T	tripod mounting bracket
CBL-XEC2-IO-CONN-0M12	0.12m cable for xEC2 IO connector, 30 pins, pig tale cable
CBL-XEC2-CAMIO-CONN-0M12	0.12m cable for xEC2 Camera GPIO connector, 40 pins, pig tale cable

Table 1-3, order info – part-#

2. TX2CB-MAIN – carrier board

The TX2CB-MAIN board is the main carrier board and provides the standard interfaces of the TX2. This board also contains the power supply logic and the IMU.

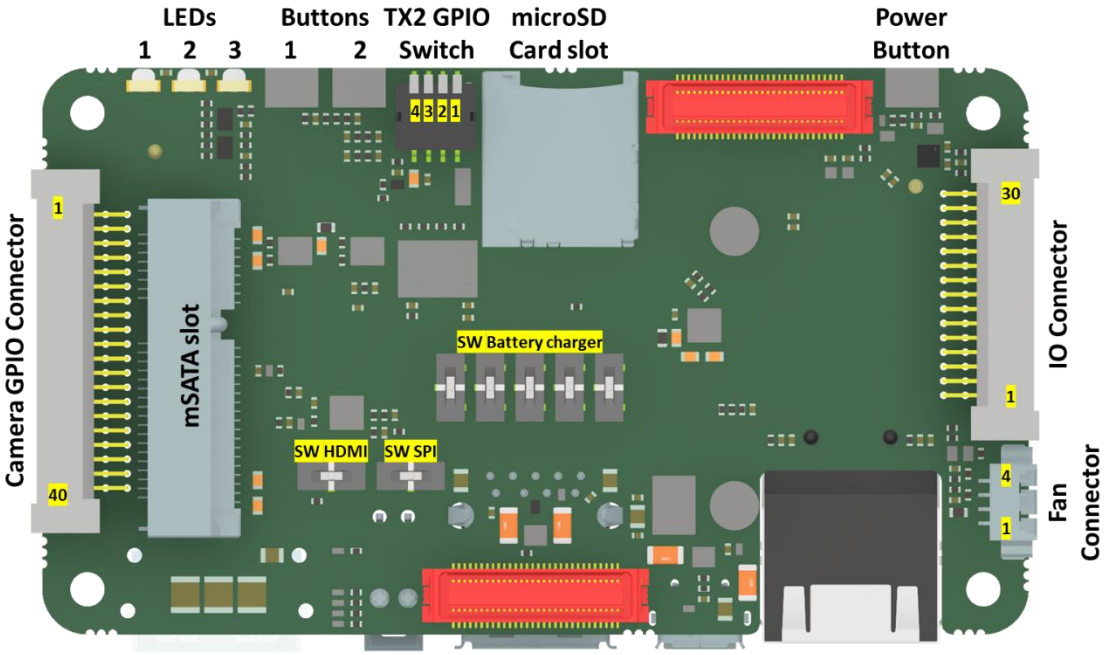


Figure 2-1, TX2CB-MAIN, upper side - components

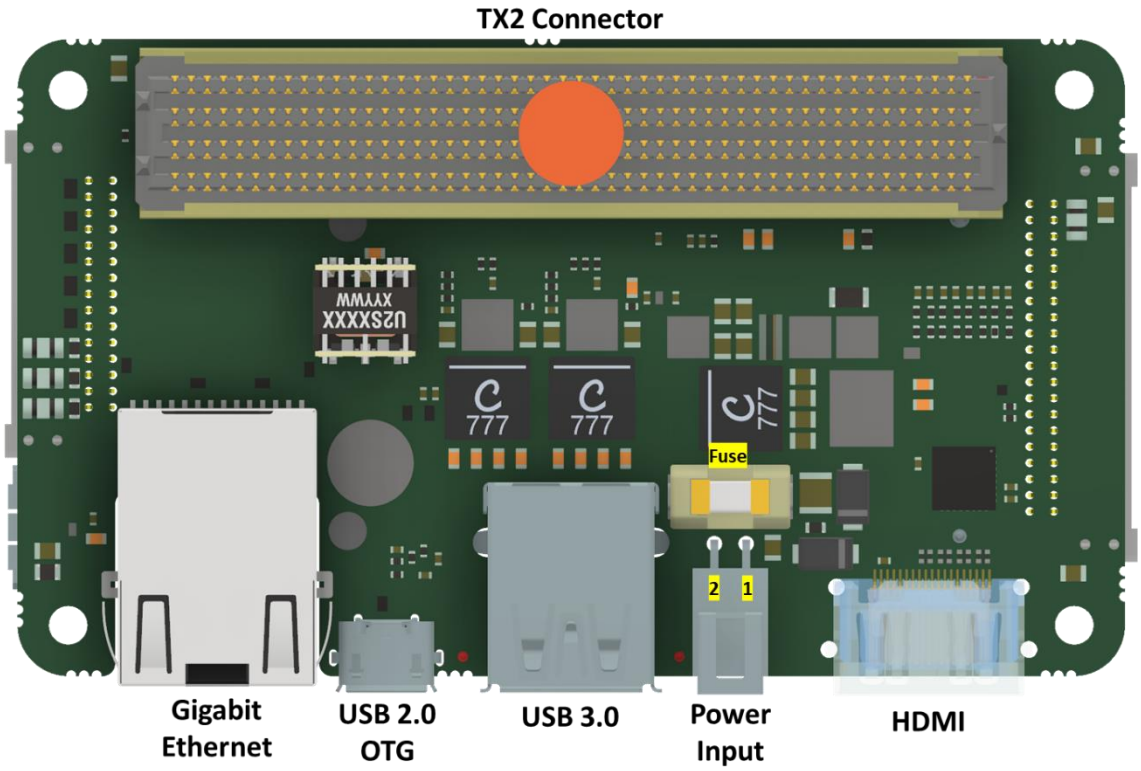


Figure 2-2, TX2CB-MAIN, lower side - components

2.1. HDMI display connector

The HDMI port is connected to the HDMI output of the NVIDIA Jetson TX2. An NXP Semiconductors IP4786CZ32 interface ESD and overcurrent protection chip is interconnected.

2.1.1. HDMI switch

This switch can be used to configure the HDMI port.

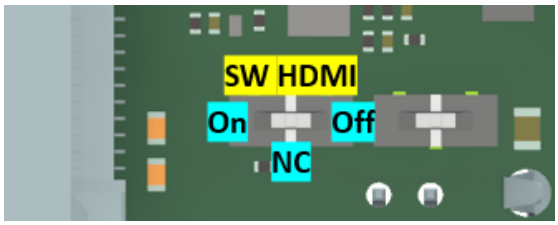


Figure 2-3, TX2CB-MAIN, HDMI switch

The switch has three different positions:

Position	Description
ON	HDMI port enabled
NC	Not connected
OFF	HDMI port disabled

Table 2-1, TX2CB-MAIN, HDMI settings

2.2. Power Input

The power input is a 2 pin male angled header connector:

Connector	Molex Nano-Fit Header, 1053131202
Mating parts	0451300201, (socket to socket, 15cm), 0451300203, (socket to socket, 30cm), 0451300210, (socket to socket, 100cm), XIMEA Socket to Barrell Adapter OD5.5/ID2.1

Table 2-2, TX2CB-MAIN, Power input Connector, parts

Pin	Description
1	VCC_IN
2	GND

Table 2-3, TX2CB-MAIN, Power input Connector, pin description

Input voltage level: nominal +12 V (+7 V to +19 V), max 8A, with Undervoltage/Overvoltage/Reverse Supply Protection.

A power cable 5.4 xEC2 Power cable is supplied with the xEC2 (XIMEA Socket to Barrell Adapter OD5.5/ID2.1).

As an alternative to this power input connector, the operating current can also be applied to pins 1 and 2 (VCC_IN) and pins 4 and 6 (GND) of the IO Connector or to battery pins 9 and 10 (VCC-BAT) of the IO Connector.

2.2.1. Fuse

VCC_IN protected by 8A/125V Fuse in Fuse-Holder. Replacement Fuse: 0451008.MRL

2.3. USB3.0

Standard Jetson TX2 USB3.0 port, USB Type-A connector.

2.4. USB2.0 OTG

Standard Jetson USB2.0 OTG port, USB micro-AB connector.

2.5. Gigabit Ethernet port

Standard Gigabit LAN RJ45 port.

2.6. Fan Connector

4 pin male header connector, angled.

Connector	Molex PicoBlade Header 053261-0471
Compatible active heat sink	DCV-01672-N2-GP

Table 2-4, TX2CB-MAIN, Fan connector, parts

Pin	Description
1	GND
2	+ 5.0 V
3	TACH
4	PWM

Table 2-5, TX2CB-MAIN, Fan Connector, pin description

Note: Setting TX2 GPIO14 pin high forces PWM to 0 and shuts down the fan.

2.7. microSD-card slot

microSD slot connected to Jetson TX2 microSD port.

2.8. mSATA slot

mSATA slot connected to Jetson TX2 mSATA port.

2.9. Buttons

Three buttons can directly affect the status of TX2 pins:

Button	Function / description	TX2 Pin#
1	GPIO8	H13
2	GPIO9	G14
Power	TX2 POWER_BTN#	B50

Table 2-6, TX2CB-MAIN, TX2CB-MAIN, buttons

2.10. LEDs

Three LEDs indicate various TX states:

LED	Function / description	TX2 Pin#
1 RED	GPIO17	B9
1 GREEN	GPIO18	B10
2 RED	GPIO13	B22
2 GREEN	GPIO16	A10
3 RED	GPIO19	F2
3 GREEN	GPIO20	H3

Table 2-7, TX2CB-MAIN, TX2CB-MAIN, buttons

2.11. TX2 GPIO Switch

The 4 On / Off dip switches can directly affect the status of TX2 pins:

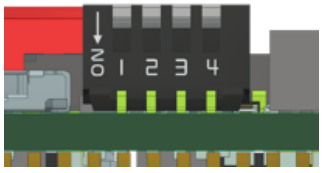


Figure 2-4, TX2CB-MAIN, TX2 GPIO Switch

Switch	Function / description	TX2 Pin#
1	GPIO10	B20
2	GPIO11	B19
3	GPIO12	B21
4	TX_FORCE_RECOV#	E1

Table 2-8, TX2CB-MAIN, TX2 GPIO Switch

2.12. Battery charger switches

The XEC2-MAIN board has configurable battery charger controller with automatic power hot swap functionality. Battery chemistry and cell count can be conveniently configured by dedicated DIP switches. Further settings can be configured using I2C interface connected to TX2 module.

The Analog Devices Multi-Chemistry Battery charger controller LTC4015 is used.

The battery can be connected to pins 9 and 10 (VCC_BAT) and 4 and 6 (GND) of the IO connector.

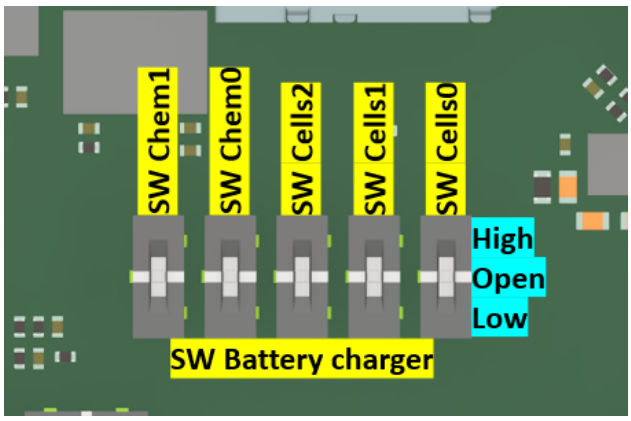


Figure 2-5, TX2CB-MAIN, battery charger switches

The various options to connect battery packs and the related switch settings are listed in the LTC4015 appendix (10 Appendix: Analog Devices Battery Charger LTC4015).

2.13. IO Connector

30 pin male header connector, 2 rows, angled.

Connector	Samtec TigerEye TFM Header TFM-115-01-S-D-RE1-WT
Mating parts	SFSD-15-28-H-05.00-SR, (socket to lose wires, 5”), SFSD-15-28-H-10.00-SR, (socket to lose wires, 10”), SFSD-15-28-H-10.00-DR-NDX, (socket to socket, 10”) Cables 2.9A per pin, 28AWG

Table 2-9, TX2CB-MAIN, IO Connector, parts

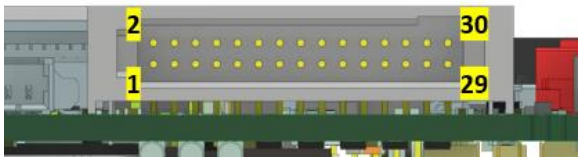


Figure 2-6, TX2CB-MAIN, IO Connector, pinout

Pin	Description	TX2 pin	Pin Type
1	VCC_IN		
2	VCC_IN		
3	+5V0		
4	GND		
5	+3V3		

6	GND		
7	+1V8		
8	VDD_RTC	A50	
9	VCC_BAT		
10	VCC_BAT		
11	GPIO0	G8	CMOS 1.8V
12	GPIO1	F7	CMOS 1.8V
13	GPIO2	H8	CMOS 1.8V
14	GPIO3	H7	CMOS 1.8V
15	GPIO4	G7	CMOS 1.8V
16	UART0_RTS#	G11	CMOS 1.8V
17	UART0_CTS#	H11	CMOS 1.8V
18	UART0_RX	G12	CMOS 1.8V
19	UART0_TX	H12	CMOS 1.8V
20	UART1_TX	D9	CMOS 1.8V
21	UART1_RX	D10	CMOS 1.8V
22	SPI2_MISO	H15	1.8V / 3.3V
23	SPI2_CLK	H14	1.8V / 3.3V
24	SPI2_MOSI	G15	1.8V / 3.3V
25	SPI2_CS0#	G16	1.8V / 3.3V
26	SPI2_CS1#	F16	1.8V / 3.3V
27	I2C_GP1_3V3_CLK	A21	
28	I2C_GP1_3V3_DAT	A20	
29	I2C_GP0_1V8_CLK	E15	
30	I2C_GP0_1V8_DAT	D15	

Table 2-10, TX2CB-MAIN, IO Connector, pin description

Component	Description
PTC Fuse	+5V0, +3V3, +1V8 protected with 350mA PTC (FEMTOSMDC035F-02).
ESD	GPIO, UART, SPI, I2C protected with TPD4F202YFUR
SPI2 Level	SPI2 Bus Voltage Level selectable by SPI voltage switch Level Translator used: SN74AVC4T234.

Table 2-11, TX2CB-MAIN, IO Connector – additional info

2.13.1. SPI voltage switch

This switch can be used to configure the SPI Voltage level port (IO Connector, pins 22 – 26)

Figure 2-7, TX2CB-MAIN, SPI Voltage switch

The switch has three different positions:

Position	Description
1V8	1.8 V
NC	Not connected
3V3	3.3 V

Table 2-12, TX2CB-MAIN, SPI Voltage settings

2.14. Camera GPIO Connector

40 pin male header connector, 2 rows, angled.

Connector	Samtec TigerEye TFM Header TFM-120-01-S-D-RE2-WT
Mating parts	SFSD-20-28-H-05.00-SR, (socket to loose wires, 5”) SFSD-20-28-H-10.00-SR, (socket to loose wires, 10”) SFSD-20-28-H-10.00-DR-NDX, (socket to socket, 10”) Cables 2.9A per pin, 28AWG

Table 2-13, TX2CB-MAIN, Camera GPIO Connector, parts

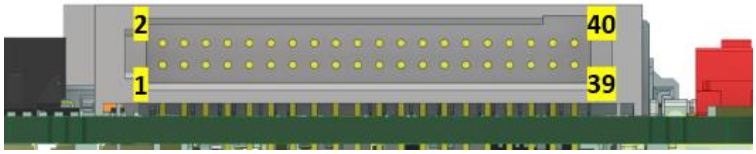


Table 2-14, TX2CB-MAIN, Camera GPIO Connector, pinout

2.14.1. Generic Pins

Pin	Description	Pin Type
1	ISO_5V0	Power
2	ISO_5V0	Power
3	ISO_GND	GND
4	ISO_GND	GND

Table 2-15, TX2CB-MAIN, Camera GPIO Connector, pin description, generic pins 1-4

The meaning of pins 5-40 depends on the connected Camera Connection Board and is described there.

Ports	Output power restrictions
GPO OC	GPO Open Collector Output limited by 36mA PTC (PRG18BB330MB1RB).
GPO 5V	Isolated 5V0 power rail is shared by all ISO_5V0 GPOs and limited to total of 350mA by FEMTOSMDC035F-02 PTC.

Table 2-16, TX2CB-MAIN, Camera GPIO Connector – output power restrictions

2.15. IMU

9-axis Absolute orientation sensor IMU ACCEL/GYRO/MAG I2C 28LGA from Bosch Sensortec, part# BNO055.

The IMU is connected to the Jetson SoC via the I^2C bus.

3. TX2CB-CONN-4P-X2G2 – camera board

On top of the camera board are the connectors for the cameras (Cam1 – Cam 7) and the NVMe SSD.

There is also a switch for configuring the trigger input for each camera port (SW C1 – SW C7).

The switch "SW SSD" is used to configure the NVMe SSD port.

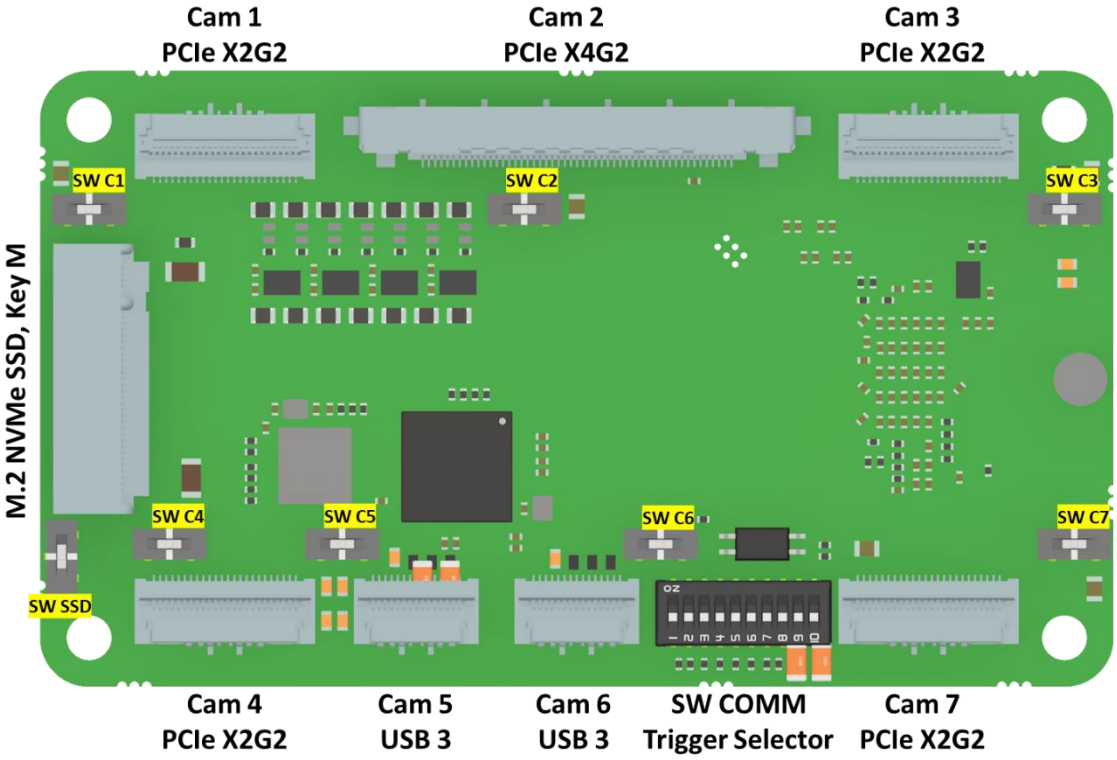


Figure 3-1, TX2CB-CONN-4P-X2G2, components

3.1. USB3 Ports

Cam 5 and Cam 6 are 2 USB3.1 Gen 1 flex cable connectors, cable orientation parallel to the board surface. These cameras are input to the Jetson via the dedicated USB3 host controller IC and PCIe switch incorporated into the device. XIMEA proprietary pinout with:

- Power for attached devices (XIMEA cameras)
- USB3.1 Gen 1, 5 GBit/s bandwidth
- IO wires

Please note *7 USB3 ports – Connectors, Cabling* for more details.

3.2. PCIe X2G2 Ports

Cam 1, Cam 3, Cam 4 and Cam 7 are flex cable connectors, 2 lanes PCIe Gen2 each, cable orientation parallel to the board surface. These cameras are input to the Jetson via the PCIe switch incorporated into the device. XIMEA proprietary pinout with:

- Power for attached devices (XIMEA cameras)
- 2 lanes, PCIe Gen 2, 10 GBit/s bandwidth
- IO wires

Please note 8 *PCIe ports – Connectors, Cabling* for more details.

3.3. PCIe X4G2 Port

Cam 2 is a flex cable connector, 4 lanes PCIe Gen2 each, cable orientation parallel to the board surface. This camera is input to the Jetson via the PCIe switch incorporated into the device. XIMEA proprietary pinout with:

- Power for attached devices (XIMEA cameras)
- 4 lanes, PCIe Gen 2, 20 GBit/s bandwidth
- IO wires

Please note 8 *PCIe ports – Connectors, Cabling* for more details.

3.4. NVMe SSD Port

The M.2 NVMe SSD port, Key M codes can be used to a M.2 NVMe SSD to store data. The PCIe lanes used to drive the SSDs are input through the PCIe switch to the Jetson.

The form factor of the supported SSDs is NVMe M.2, Key M coded, 4 lanes PCIe with a form factor of up to 2280 (80 mm long).

3.5. Camera trigger input switches

The 7 switches "SW C1" – "SW C7" are used to select which signals are connected to the optically isolated trigger input pin of each camera port (Cam 1 – Cam 7).

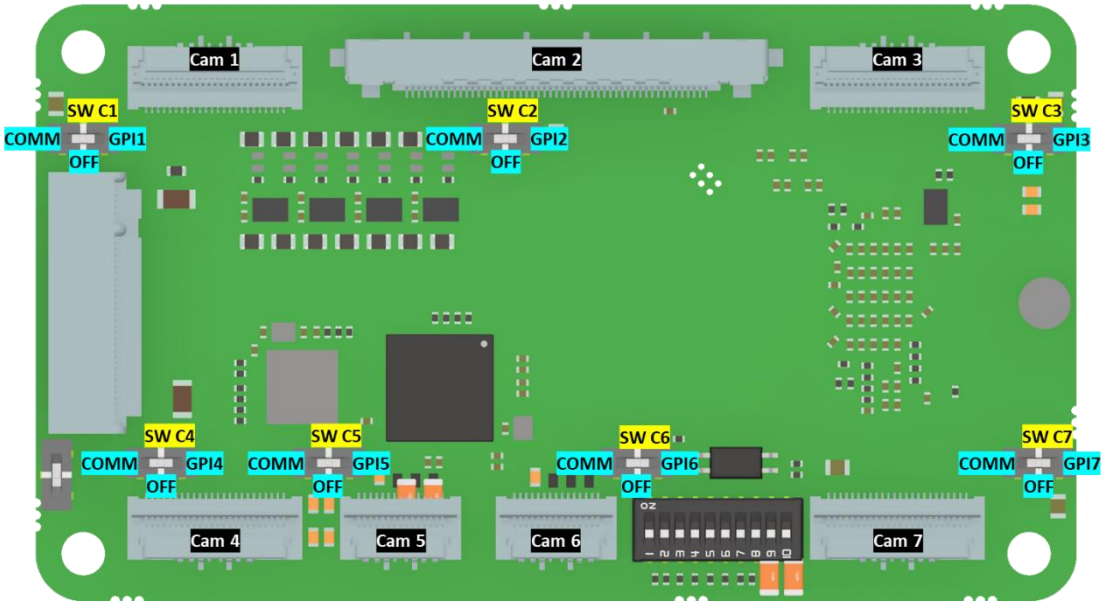


Figure 3-2, TX2CB-CONN-4P-X2G2, Camera trigger input switches

Each switch has three possible settings:

Position	Description
COMM	Common Input signal
OFF	Not connected
GPI n	Individual Input pin on Camera GPIO Connector

Table 3-1, TX2CB-CONN-4P-X2G2, Camera trigger input switch settings

Details are explained in *4 Camera trigger system / synchronization*

3.6. Camera common trigger input selector

The Common input trigger selector determines which possible input signal is applied to the COMM position of the camera input trigger switches “SW C1” – “SW C7”.

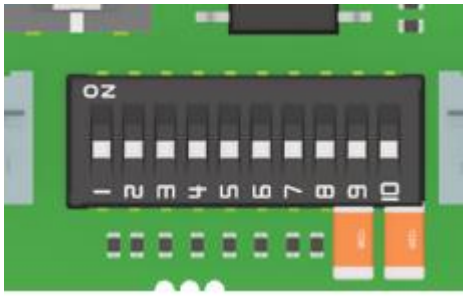


Figure 3-3, TX2CB-CONN-4P-X2G2, Camera common trigger input selector

It is a switch with 10 positions. Each of the individual positions can have two values:

Position	Description
ON	Switch closed
OFF	Switch not closed

Table 3-2, TX2CB-CONN-4P-X2G2, Camera common trigger input selector settings

Details are explained in *4 Camera trigger system / synchronization*

3.7. USB 3.1 Gen 2 Controller

AS Media ASM3142 USB3 host controller

3.8. PCIe switch

PCIe Switch, PLX technologies, PEX8725

3.9. Camera GPIO-Connector, Meaning of the pins

The meaning of most of the pins of the Camera GPIO connector (2.14 Camera GPIO Connector) depends on the connected camera board.

Pin function in combination with camera board TX2CB-CONN-4P-X2G2.

Pin	Description	Pin Type
1	ISO_5V0	Power
2	ISO_5V0	Power
3	ISO_GND	GND
4	ISO_GND	GND
5	CAM12_GPI	Extern master trigger input
6 -9		Not used
10	CAM7_GPI	Input
11	CAM6_GPI	Input
12	CAM5_GPI	Input
13	CAM4_GPI	Input
14	CAM3_GPI	Input
15	CAM2_GPI	Input
16	CAM1_GPI	Input
17 - 26		Not used
27	CAM7_GPO_OC	Output Open Collector
28	CAM7_GPO_5V	Output Push-Pull
29	CAM6_GPO_OC	Output Open Collector
30	CAM6_GPO_5V	Output Push-Pull
31	CAM5_GPO_OC	Output Open Collector
32	CAM5_GPO_5V	Output Push-Pull
33	CAM4_GPO_OC	Output Open Collector
34	CAM4_GPO_5V	Output Push-Pull
35	CAM3_GPO_OC	Output Open Collector
36	CAM3_GPO_5V	Output Push-Pull
37	CAM2_GPO_OC	Output Open Collector
38	CAM2_GPO_5V	Output Push-Pull
39	CAM1_GPO_OC	Output Open Collector
40	CAM1_GPO_5V	Output Push-Pull

Table 3-3, TX2CB-MAIN, Camera GPIO Connector, pin description in combination with TX2CB-CONN-4P-X2G2

4. Camera trigger system / synchronization

All cameras connected to the camera connections Cam1 - Cam7 of the xEC2 embedded system can be triggered / synchronized and used as trigger masters for connected devices / cameras.

The pins on the Camera GPIO Connector can be used to connect any combination of cameras to trigger groups.

Each camera can be triggered individually by external signals.

4.1. Camera Input-/Output signals

The (first) optically isolated GPIO ports are used as trigger input or output of the cameras:

Cam Port	Cam Type	Connected GPI port	Connected GPO port
Cam 1	PCIe X2G2	IN1	OUT1
Cam 2	PCIe X4G2	IN1	OUT1
Cam 3	PCIe X2G2	IN1	OUT1
Cam 4	PCIe X2G2	IN1	OUT1
Cam 5	USB 3.1	xiQ: GPI, xiC, xiX: IN1	xiQ: GPO, xiC, xiX: OUT1
Cam 6	USB 3.1	xiQ: GPI, xiC, xiX: IN1	xiQ: GPO, xiC, xiX: OUT1
Cam 7	PCIe X2G2	IN1	OUT1

Table 4-1, Used camera trigger pins

The trigger outputs of the cameras used are open collector outputs.

To the outside (Camera GPIO Connector) the open collector outputs as well as levels pulled to 5V are available.

The outputs with a 5V level can be used to trigger other cameras directly.

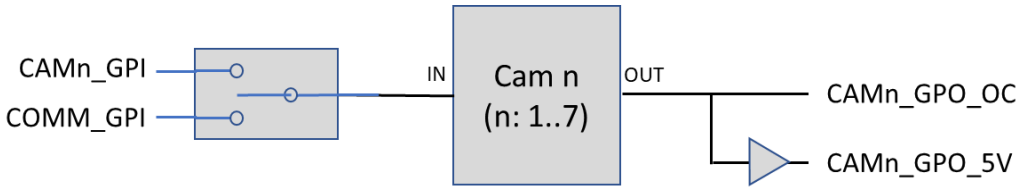


Figure 4-1, simplified camera trigger IO

For each camera, the camera trigger input switch can be used to define which signal is to be used at the GPI: Please note *3.5 Camera trigger input switches :*

- CAMn_GPI are the input signals on the Camera GPIO Connector (*2.14 Camera GPIO Connector*)
- Common trigger signal COMM_GPI

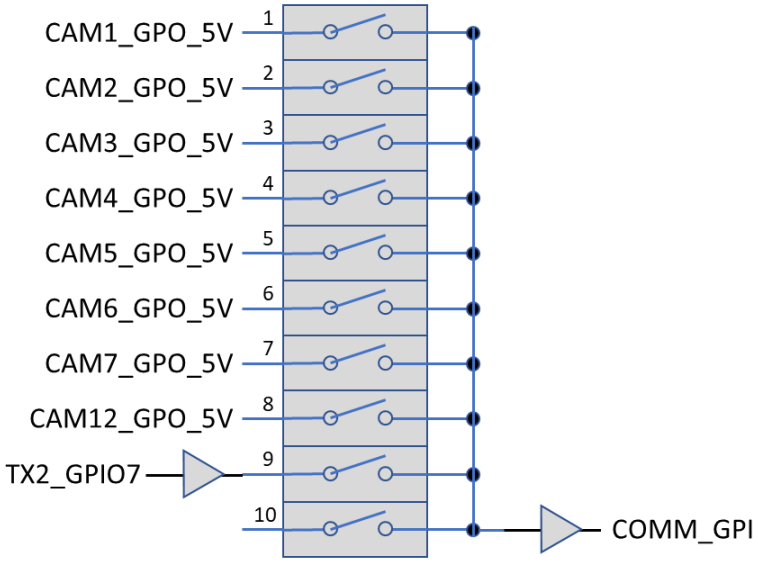
4.2. Common Input signal COMM_GPI

The xEC2 system provides a common trigger source (COMM) that can be used to synchronize the cameras.

The Common input trigger selector *(3.6 Camera common trigger input selector)* can be used to determine which trigger source is to be used as this common trigger source.

Input signals can be:

- Any of the 7 CAMn_GPO_5V signals
- External trigger source (Pin CAM12_GPI_ISO) at the Camera GPIO Connector (*2.14 Camera GPIO Connector*)
- Jetson GPIO port TX2_GPIO7 (TX2 Pin B23)



5. Scope of delivery / Accessories

The scope of delivery when ordering the product xEC2 is:

- xEC2 board stack as visualized in 1.2 Components
  - Camera breakout board – TX2CB-CONN-4P-X2G2
  - Main carrier board – TX2CB-MAIN
  - NVIDIA Jetson TX2 / TX2i SoC embedded computer
  - Tripod baseplate
  - Screws and standoffs
- Power cable (5.4 xEC2 Power cable)

5.1. XEC2-FAN-COOLER-KIT

XEC2-FAN-COOLER-KIT is an heatsink with an active fan (sold separately). The fan can be connected to the XEC2-MAIN board via a 4-pin cable, see 2.6 Fan Connector. The fan speed is controlled by the TX2 as needed.

The kit includes 4 screws to fix the heatsink to the xEC2 baseplate or directly to the TX2 rear side.

(© auvidea.eu)

Figure 5-1, XEC2-FAN-COOLER-KIT

5.2. PSU-GSM60B12-P1J

PSU-GSM60B12-P1J is a AC-DC desktop power supply (sold separately).

Output: 12V DC at 5A, up to 60W: AC 2-pole IEC320-C8 inlet, OD5.5/ID2.1 DC connector

Part of the kit is a power cord (EU or US).

5.3. PSU-GSM60A15-P1J

PSU-GSM60A15-P1J is a AC-DC desktop power supply (sold separately).

Output: 15V DC at 4A, up to 60W: AC 3 pin IEC320-C14 input socket, OD5.5/ID2.1 DC connector

Part of the kit is a power cord (DE).

5.4. xEC2 Power cable

A power cable is supplied with the xEC2 to connect the power supplies 5.2 PSU-GSM60B12-P1J and 5.3 PSU-GSM60A15-P1J to the power input 2.2 Power Input.

Figure 5-2, xEC2 power cable

5.5. MECH-60MM-BRACKET-T

MECH-60MM-BRACKET-T is a tripod mounting bracket that can be screwed to the XEC2-baseplate (sold separately). M4 screws are part of the delivery.

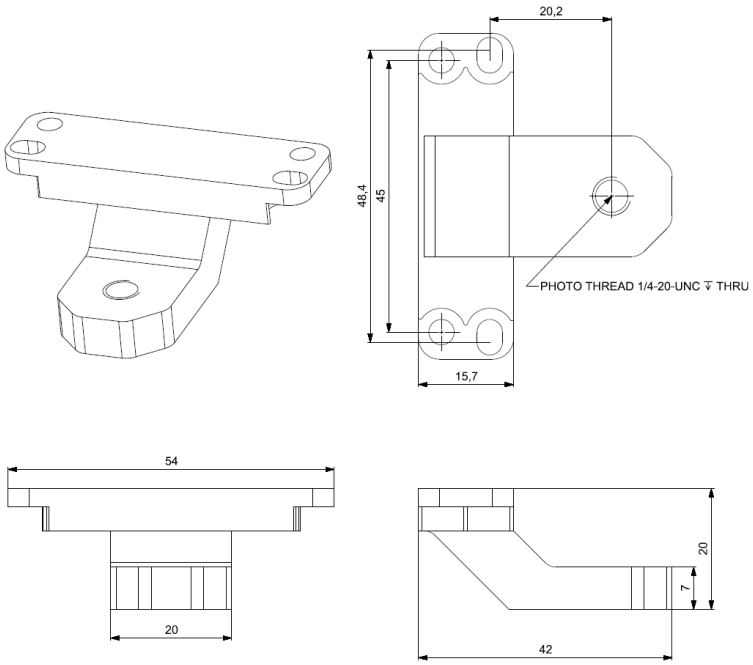


Figure 5-3, MECH-60MM-BRACKET-T, dimensional drawing

5.6. CBL-XEC2-IO-CONN-0M12

CBL-XEC2-IO-CONN-0M12 is a 0.12m (5”) cable for the xEC2 IO connector (2.13 IO Connector) with 30 pig tale wires (sold separately).

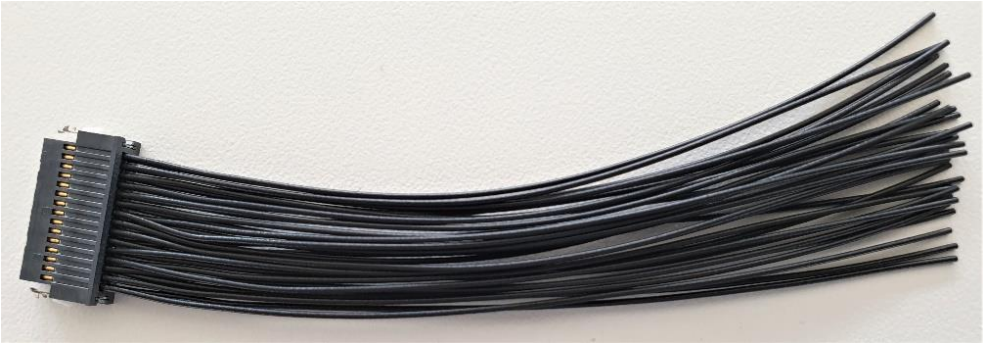


Figure 5-4, CBL-XEC2-IO-CONN-0M12

5.7. CBL-XEC2-CAMIO-CONN-0M12

CBL-XEC2-CAMIO-CONN-0M12 is a 0.12m (5”) cable for the xEC2 Camera GPIO connector (2.14 Camera GPIO Connector) with 40 pig tale wires (sold separately).

Figure 5-5, CBL-XEC2-CAMIO-CONN-0M12

6. Compatible cameras

6.1. USB-3 cameras

Compatible to the USB 3 flex cable connectors are various XIMEA cameras:

6.1.1. xiQ / xiSpec cameras

All xiQ cameras with CMV2000 and CMV4000 sensors are available as flex-ribbon variants and xEX2 compatible as well as all xiSpec cameras.

https://www.ximea.com/files/brochures/xiQ-USB3-Vision-cameras-2017-brochure-HQ.pdf

https://www.ximea.com/files/brochures/xiSpec-Hyperspectral-HSI-cameras-2017-brochure-HQ.pdf

http://www.ximea.com/downloads/usb3/manuals/xiq_technical_manual.pdf

6.1.2. xiC cameras

All xiC cameras are available as flex-ribbon variants and xEX2 compatible.

https://www.ximea.com/files/brochures/xiC-USB3_1-Sony-CMOS-Pregius-cameras-brochure-HQ.pdf

http://www.ximea.com/downloads/usb3/manuals/xic_technical_manual.pdf

6.2. PCIe cameras

Compatible to the PCIe flex cable connectors are various XIMEA cameras:

6.2.1. xiX cameras

All xiX cameras with a 2 lane PCIe Gen 2 interface are available as flex-ribbon variants and xEX2 compatible.

https://www.ximea.com/files/brochures/xiX-OEM-cameras-for-integration-2017-brochure-HQ.pdf

http://www.ximea.com/downloads/cb/manuals/xix_technical_manual.pdf

6.2.2. xiSpec cameras

All xiSpec cameras can be ordered in a special PCIe version with a flex cable 2 lane PCIe Gen 2 interface.

https://www.ximea.com/files/brochures/xiSpec-Hyperspectral-HSI-cameras-2017-brochure-HQ.pdf

7. USB3 ports – Connectors, Cabling

7.1. USB 3.1 Gen 1 + GPIO Connector pinning

The pinning of the USB3 / IO ports on the xEC2 is:

Pin	Signal	Technical description
15	GND	Ground for power return and for SuperSpeed signal return
14	SSRX-	SuperSpeed receiver differential pair; Accepted SSRX+
13	SSRX+	SuperSpeed receiver differential pair; Accepted SSRX-
12	GND	Ground for power return and for SuperSpeed signal return
11	SSTX+	SuperSpeed transmitter differential pair; Accepted SSTX-
10	SSTX-	SuperSpeed transmitter differential pair; Accepted SSTX+
9	GND	Ground for power return and for SuperSpeed signal return
8	D+	USB 2.0 differential pair
7	D-	USB 2.0 differential pair
6	GND	Ground for power return and for SuperSpeed signal return
5	VBUS	+5V Power input
4	VBUS	+5V Power input
3	Trigger/sync digital Output (GPO)	Open collector NPN, opto-isolated
2	Common pole (IO Ground)	
1	Trigger/sync digital Input (GPI)	Current limited (current sink) input, opto-isolated
Ground pins	SGND	Shield of FPC cable connected to shield of host controller

Table 7-1, USB + GPIO connector Pin Assignment

7.2. Connectors

The USB3 / IO connectors are:

Molex 502231-1530

7.3. USB3 - FPC cable

Some flat ribbon USB3 cameras were supplied with a polarized custom cable (PN: CBL-MQ-FL-xxx). Camera side is laser marked "CAM" and xEC2 / break-out-board side is marked "BOB".

The FPC cable must be connected to the camera and the computer / break-out-board or carrier-board in the correct orientation.

The newer generation of these cables (PN: CBL-USB3FLEX-xxx) is NOT polarized and either end can be used for the camera or xEC2 connector.

Cables PN: CBL-MQ-FL-xxx:
The camera and / or the computer interface can be destroyed in case of wrong cabling.

Turn power off and unlock the connector before inserting / detaching the cable to avoid any damage.

Figure 7-1, xiQ/xiC FPC cable, PN: CBL-MQ-FL-xxx

Figure 7-2, xiQ/xiC FPC cable, PN: CBL-USB3FLEX-xxx

Important note:
The EMI/EMC performance should be evaluated by customer. The customer is liable for compliance to FCC and/or any other national regulations of device(s) containing the subassembly.

7.3.1. Cable orientation

The basic orientation of the FPC cables in the connector can be seen in the following diagram:

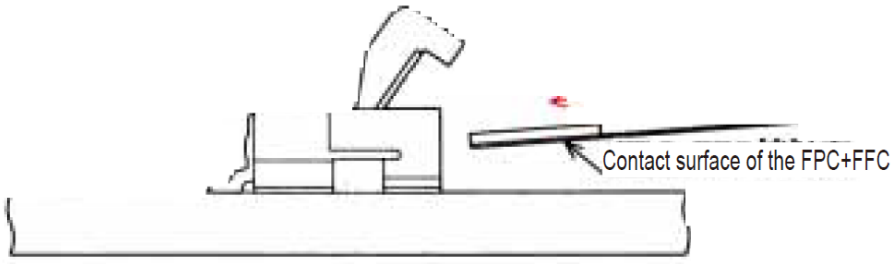


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Figure 7-3, FPC-cable orientation in the connector

7.3.2. Camera side

The camera side of the FPC cables CBL-MQ-FL-xxx is laser marked “CAM”:

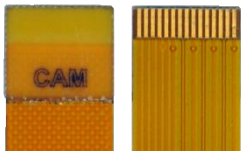


Figure 7-4, xiQ/xiC cable, PN: CBL-MQ-FL-xxx – camera side

This CAM-side of the cable must be connected to the camera:

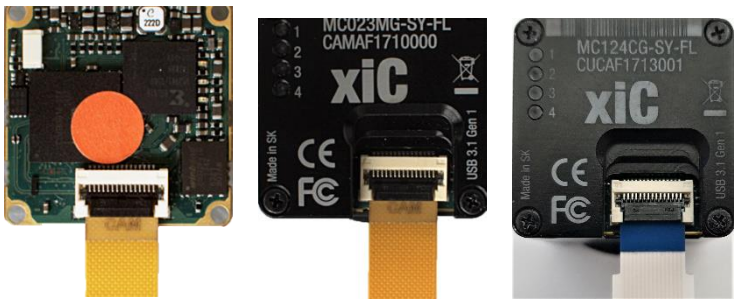


Figure 7-5, xiQ (left) and xiC (right) – camera side, correct FPC cabling

7.3.3. Break-out-board / xEC2 embedded computer side

The “computer” side of the FPC- cables CBL-MQ-FL-xxx is laser marked “BOB” (break-out-board):

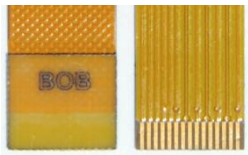


Figure 7-6, xiQ/xiC cable, PN: CBL-MQ-FL-xxx – break-out-board side

This BOB-side of the cable must be connected to the xEC2 / break-out-box.

8. PCIe ports – Connectors, Cabling

8.1. PCIe x2 Gen 2 and GPIO pinning

The pinning of the PCIe ports on the xEC2 is:

Pin	Name	Level	Description
24	GND		External grounds for power supply, PCIe and non-isolated I/O
23	PCIe_REFCLK_P		
22	PCIe_REFCLK_N		
21	GND		External grounds for power supply, PCIe and non-isolated I/O
20	PCIe_PERP_1		
19	PCIe_PERN_1		
18	GND		External grounds for power supply, PCIe and non-isolated I/O
17	PCIe_PERP_0		
16	PCIe_PERN_0		
15	GND		External grounds for power supply, PCIe and non-isolated I/O
14	PCIe_PETP_1		
13	PCIe_PETN_1		
12	GND		External grounds for power supply, PCIe and non-isolated I/O
11	PCIe_PETP_0		
10	PCIe_PETN_0		
9	GND		External grounds for power supply, PCIe and non-isolated I/O
8	PCIe_RST_N		PCIe reset signal active low
7	PWR	12-24V	Power Supply Input
6	PWR		
5	INOUT1	LVTTL (3.3, 50µA)	non-isolated Input/Output
4	INOUT2	LVTTL (3.3, 50µA)	non-isolated Input/Output
3	IN1		Opto-isolated Input 1
2	IN_OUT_GND		Common ground for opto-isolated IO
1	OUT1		Opto-isolated Output 1

Table 8-1, PCIe / IO connector pin assignments

8.1.1. Connectors

The PCIe / IO connectors are:

Molex 502231-2430

8.1.2. PCIe Gen 2, 2 lanes - FPC cable

Some flat ribbon PCIe cameras were supplied with a polarized custom cable (PN: CBL-MX-X2G2-xxx). Camera side is laser marked "CAM" and xEC2 / break-out-board side is marked "BOB".

The FPC cable must be connected to the camera and the computer / break-out-board or carrier-board in the correct orientation.

The newer generation of these cables (PN: CBL-PCIEFLEX-X2G2-xxx) is NOT polarized and either end can be used for the camera or xEC2 connector.

Cables PN: CBL-MX-X2G2-xxx:
The camera and / or the computer interface can be destroyed in case of wrong cabling.

Turn power off and unlock the connector before inserting / detaching the cable to avoid any damage.

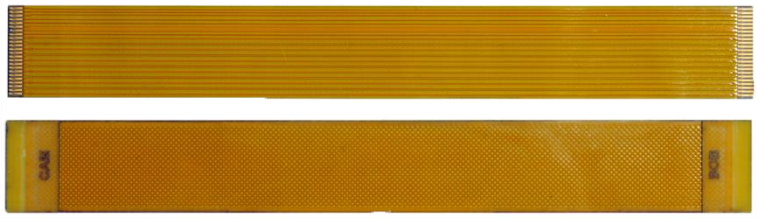


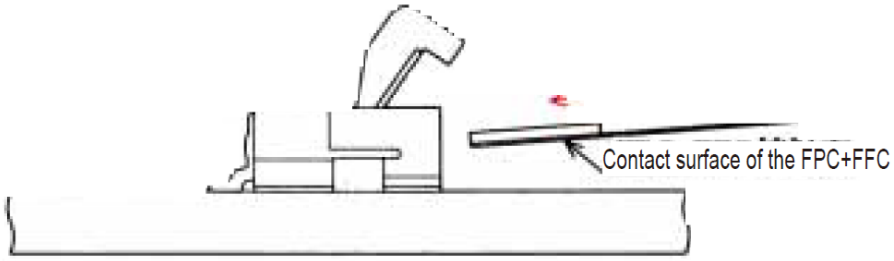
Figure 8-1, xiX X2G2 FPC cable, PN: CBL-MX-X2G2-xxx

Figure 8-2, xiX X2G2 FPC cable, PN: CBL-PCIEFLEX-X2G2-xxx

Important note:
The EMI/EMC performance should be evaluated by customer. The customer is liable for compliance to FCC and/or any other national regulations of device(s) containing the subassembly.

8.1.3. Cable orientation

The basic orientation of the FPC cables in the connector can be seen in the following diagram:



© Hirose

Figure 8-3, FPC-cable orientation in the connector

8.1.4. Camera side

The camera side of the FPC cables CBL-MX-X2G2-xxx is laser marked “CAM”:

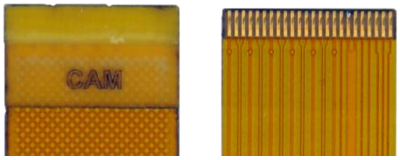


Figure 8-4, xiX X2G2 cable, PN: CBL-MX-X2G2-xxx – camera side

This CAM-side of the cable must be connected to the camera:

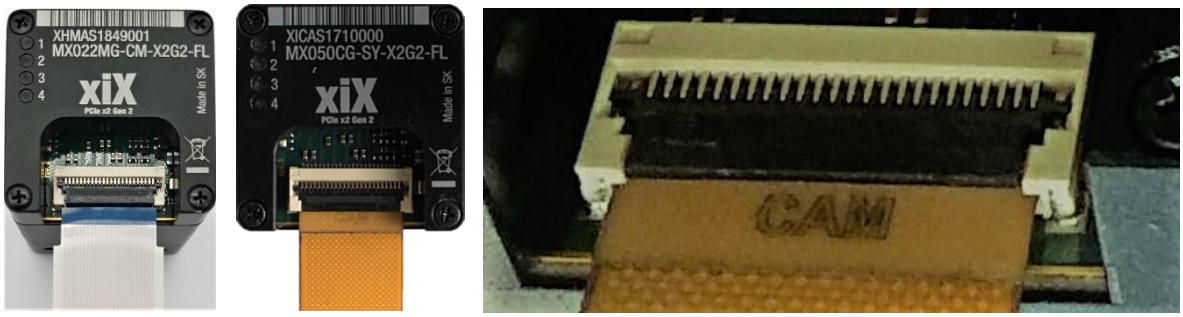


Figure 8-5, xiX X2G2 – camera side, correct FPC cabling

8.1.5. PCIe adapters / embedded computer side

The “computer” / adapter side of the FPC-cables CBL-MX-X2G2-xxx is laser marked “BOB” (break-out-board):

Figure 8-6, xiX X2G2 cable, PN: CBL-MX-X2G2-xxx – break-out-board side

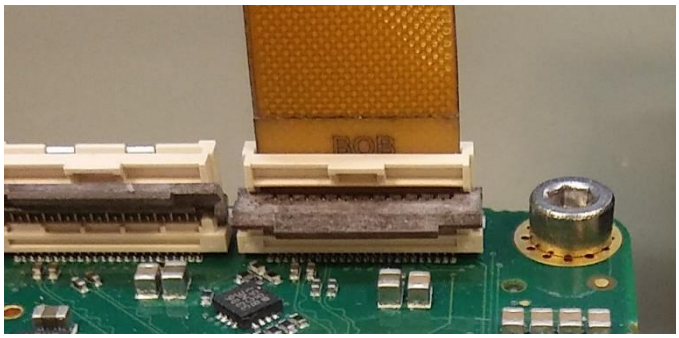


Figure 8-7, xiX X2G2 – break-out-board side, correct FPC cabling

This BOB-side of the cable must be connected to the xEC2 board.

8.2. PCIe x4 Gen 2 and GPIO pinning

Turn power off and unlock the connector before inserting / detaching the cable to avoid any damage.

The pinning of the PCIe ports on the xEC2 is:

Pin	Name	Direction	Level	Description
51	GND	-		External grounds for power supply and non-isolated I/O
50	IN1	In	(<0.8 Low; 4-24 High)	Opto-isolated Input 1
49	IN GND	-		Common ground for Opto-Isolated inputs
48	IN2	In	(<0.8 Low; 4-24 High)	Opto-isolated Input 2
47	GND	-		External grounds for power supply and non-isolated I/O
46	INOUT1	In/Out	LVTTL (3.3, 50µA)	non-isolated Input/Output
45	INOUT2	In/Out	LVTTL (3.3, 50µA)	non-isolated Input/Output
44	NC			Not Connected
43	GND	-		External grounds for power supply and non-isolated I/O
42	NC			Not Connected
41	NC			Not Connected
40	GND	-		External grounds for power supply and non-isolated I/O
39	PERp0	In		Differential PCI Express Receiver Lane

38	PERn0	In		Differential PCI Express Receiver Lane
37	GND	-		External grounds for power supply and non-isolated I/O
36	PERp1	In		Differential PCI Express Receiver Lane
35	PERn1	In		Differential PCI Express Receiver Lane
34	GND	-		External grounds for power supply and non-isolated I/O
33	PERp2	In		Differential PCI Express Receiver Lane
32	PERn2	In		Differential PCI Express Receiver Lane
31	GND	-		External grounds for power supply and non-isolated I/O
30	PERp3	In		Differential PCI Express Receiver Lane
29	PERn3	In		Differential PCI Express Receiver Lane
28	GND	-		External grounds for power supply and non-isolated I/O
27	AUX PWR	-	12-24V	Power Supply
26	AUX PWR	-	12-24V	Power Supply
25	AUX PWR	-	12-24V	Power Supply
24	GND	-		External grounds for power supply and non-isolated I/O
23	PETp0	Out		Differential PCI Express Transmitter Lane
22	PETn0	Out		Differential PCI Express Transmitter Lane
21	GND	-		External grounds for power supply and non-isolated I/O
20	PETp1	Out		Differential PCI Express Transmitter Lane
19	PETn1	Out		Differential PCI Express Transmitter Lane
18	GND	-		External grounds for power supply and non-isolated I/O
17	PETp2	Out		Differential PCI Express Transmitter Lane
16	PETn2	Out		Differential PCI Express Transmitter Lane
15	GND	-		External grounds for power supply and non-isolated I/O
14	PETp3	Out		Differential PCI Express Transmitter Lane
13	PETn3	Out		Differential PCI Express Transmitter Lane
12	GND	-		External grounds for power supply and non-isolated I/O
11	CREFCLKp	In		Differential 100 MHz Cable Reference Clock
10	CREFCLKn	In		Differential 100 MHz Cable Reference Clock
9	GND	-		External grounds for power supply and non-isolated I/O
8	CPERST#	In		PCIe PERST# active low reset signal
7	INOUT3	In/Out	LVTTL (3.3, 50µA)	non-isolated Input/Output
6	INOUT4	In/Out	LVTTL (3.3, 50µA)	non-isolated Input/Output
5	GND	-		External grounds for power supply and non-isolated I/O
4	OUT2	Out	Open collector	Opto-isolated Output 2
3	OUT GND	-	Common GND for OUT	Common ground for Opto-Isolated outputs
2	OUT1	Out	Open collector	Opto-isolated Output 1
1	GND	-		External grounds for power supply and non-isolated I/O

Table 8-2, xiX (X4G2) digital input interface

8.2.1. Connectors

The PCIe / IO connectors are:

Item	Parameter	Note
Interface connector	JAE FI-R Series 51pos connector	FI-RE51S-HF-R1500 / FI-RE51S-VF-R1300
Mating cable	JAE JF08 Series 51pos FFC cable assembly	JF08R0R051020MA

Table 8-3, xiX (X4G2) connectors

9. Additional info

9.1. Access to NVIDIA Jetson TX2

9.1.1. Network login

After connected to a network with a DHCP server and powered up for 60 seconds - try to ping on the local network 'tegra-ubuntu':

login with SSH

```
putty tegra-ubuntu
user: nvidia
pass: nvidia
```

9.1.2. XIMEA Linux API on TX2

Please note our most recent info at: https://www.ximea.com/support/wiki/apis/Linux_TX1_and_TX2_Support

The XIMEA API is pre-installed on the XEC2 Board stack.

9.1.3. Linux for Tegra (L4T) development

Valuable hints for software development for xEC2 can be found at NVIDIA (L4T 32.1) at
https://developer.nvidia.com/embedded/linux-tegra

The Jetson TX2 board connector provides access to many System GPIO. Information on GPIO controller assignment and enumeration can be found in the file tegra_186-gpio.h

9.1.4. Access info to some components of the xEC2 board stack

I2C Linux bus numbers and addresses:

LTC4015 (charger)	bus 7, address 0x68
BNO055 (gyro)	bus 8, address 0x28
I2C_GP0	bus 0
I2C_GP1	bus 1

UART Linux device names:

UART0	/dev/ttyS0
UART1	/dev/ttyTHS2

SPI2 device tree name: spi@3210000

GPIO numbers in Linux (see pinmux table and include/dt-bindings/gpio/tegra186-gpio.h):

BTN_B5	320 + 8 * 8 + 4 | GPIO8_ALS_PROX_INT	-> GPIO3_PI.04
BTN_B6	256 + 5 * 8 + 2 | GPIO9_MOTION_INT	-> GPIO3_PAA.02
SWX_B7_0	320 + 2 * 8 + 0 | GPIO10_WIFI_WAKE_AP	-> GPIO3_PC.00
SWX_B7_1	320 + 8 * 8 + 5 | GPIO11_AP_WAKE_BT	-> GPIO3_PI.05
SWX_B7_2	320 + 1 * 8 + 4 | GPIO12_BT_EN	-> GPIO3_PB.04
LED_D8_R	320 + 8 * 8 + 7 | GPIO17_MDM2AP_READY	-> GPIO3_PI.07
LED_D8_G	320 + 8 * 8 + 6 | GPIO18_MDM_COLDBOOT	-> GPIO3_PI.06
LED_D9_R	320 + 1 * 8 + 5 | GPIO13_BT_WAKE_UP	-> GPIO3_PB.05
LED_D9_G	320 + 20 * 8 + 1 | GPIO16_MDM_WAKE_AP	-> GPIO3_PY.01
LED_D10_R	320 + 9 * 8 + 6 | GPIO19_AUD_RST	-> GPIO3_PJ.06
LED_D10_G	320 + 9 * 8 + 5 | GPIO20_AUD_INT	-> GPIO3_PJ.05
GPIO0	320 + 17 * 8 + 0 | GPIO0_CAM0_PWR#	-> GPIO3_PR.00
GPIO1	320 + 13 * 8 + 2 | GPIO1_CAM1_PWR#	-> GPIO3_PN.02
GPIO2	320 + 17 * 8 + 5 | GPIO2_CAM0_RST#	-> GPIO3_PR.05
GPIO3	320 + 17 * 8 + 1 | GPIO3_CAM1_RST#	-> GPIO3_PR.01
GPIO4	256 + 2 * 8 + 5 | GPIO4_CAM_STROBE	-> GPIO3_PV.05
GPIO7	256 + 0 * 8 + 3 | GPIO7_TOUCH_RST	-> GPIO3_PS.03

9.2. Useful links

General info is available at:

NVIDIA: http://www.nvidia.com/object/embedded-systems-dev-kits-modules.html

XIMEA https://www.ximea.com/en/products/xilab-application-specific-custom-oem/Embedded-vision-cameras-xiX

https://www.ximea.com/support/wiki/apis/Linux_TX1_and_TX2_Support

Bosch: https://ae-bst.resource.bosch.com/media/_tech/media/datasheets/BST_BNO055_DS000_14.pdf

https://ae-bst.resource.bosch.com/media/_tech/media/application_notes/BST-BNO055-AN007-00_Quick_Start_Guide.pdf

Analog Devices: https://www.analog.com/media/en/technical-documentation/data-sheets/4015fb.pdf

10. Appendix: Analog Devices Battery Charger LTC4015

LTC4015

OPERATION

Cells Selection

Number of series cells selection is made using the CELLS2, CELLS1, and CELLS0 pins. For lithium chemistries the LTC4015 allows charging of up to nine series cells. For lead-acid there are only three valid selections 3, 6 or 12 cells corresponding to 6, 12, and 24V batteries respectively. Note that number of cells multiplied by their expected maximum cell voltage during charging cannot exceed V_{IN} – 200mV. With V_{IN}/V_{SYS} limited to 35V as an upper bound for V_{BAT}, at nine cells the maximum V/cell would be 3.89V. In practice the 3.89V/cell will be lower, due to several factors including; input ideal diode drop (V_{IN} – V_{SYS}) and switcher max duty cycle. These pins should be hard wired to GND(L), $INTV_{CC}$(H), or left open (Z). The LTC4015 does not monitor or balance individual cells – the full battery stack voltage is divided by number of cells (V/cell) for simplicity only. The 4015 is not a substitute for pack protection!

NUMBER OF CELLS	CELLS2	CELLS1	CELLS0
Invalid	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	L	L	Z
5	L	Z	L
6	L	H	Z
7	L	Z	H
8	L	Z	Z
9	H	L	L
Invalid	H	L	H
Invalid	H	H	L
12*	H	H	H

* Lead-acid only

Figure 10-1, LTC4015 – cell and chemistry selection

Chemistry Selection

Chemistry selection is made using the CHEM1 and CHEM0 pins. These are three-state pins used by the LTC4015 to select of one of nine chemistry specific charging algorithms. These pins should be hard wired to GND(L), $INTV_{CC}$(H), or left open (Z).

CHEMISTRY	CHEM1	CHEM0
Li-Ion Programmable	L	L
Li-Ion 4.2V/Cell Fixed	H	H
Li-Ion 4.1V/Cell Fixed	L	Z
Li-Ion 4V/Cell Fixed	Z	L
$LiFePO_4$ Programmable	L	H
$LiFePO_4$ Fixed Fast Charge	H	Z
$LiFePO_4$ Fixed Standard Charge	Z	H
Lead-Acid Fixed	Z	Z
Lead-Acid Programmable	H	L

Li-Ion/$LiFePO_4$ Battery Charging

It is the responsibility of the user of the LTC4015 to consult with the battery manufacturer to determine the recommended charging parameters for a particular battery. Battery allowable temperature range while charging and any required charging parameter temperature coefficients also need to be considered.

Pin functions:

CHEM0: Chemistry Select Pin. Three-state pin used in combination with CHEM1 to set the battery chemistry and charge algorithm.

CHEM1: Chemistry Select Pin. Three-state pin used in combination with CHEM0 to set the battery chemistry and charge algorithm.

CELLS0: Number of Cells Select Pin. Three-state pin used in combination with CELLS1 and CELLS2 to set

the total number of battery cells.

CELLS1: Number of Cells Select Pin. Three-state pin used in combination with CELLS0 and CELLS2 to set the total number of battery cells.

CELLS2: Number of Cells Select Pin. Three-state pin used in combination with CELLS0 and CELLS1 to set the total number of battery cells.

11. Revision history

Version	Date	Notes
V1.2	09/11/2019	Weight corrected (1.5.1)

12. List of figures

13. List of tables

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